Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

A1

1. (original) A method comprising:

configuring a mode word;

detecting insertion of a medium into a drive based on the mode word; and

starting a program on the medium when the insertion is detected.

2. (original) The method of claim 1 wherein configuring the mode word comprising:

configuring the mode word in one of first, second, third, and fourth modes.

3. (original) The method of claim 1 wherein detecting the insertion comprises:

periodically polling the drive when the mode word is configured in the first mode.

4. (original) The method of claim 1 wherein detecting the insertion comprises:

servicing an interrupt indicating the insertion of the medium when the mode is configured in one of the second, third, and fourth modes.

5. (original) The method of claim 1 wherein servicing the interrupt comprises:

servicing the interrupt generated by a polling circuit in a chipset when the mode is configured in one of the second and third modes, the polling circuit detecting the insertion of the medium.

6. (currently amended) The method of claim 5 wherein servicing the interrupt comprises:

checking a status bit set by the polling circuit when the mode is configured in the second mode; ~~and~~

updating a flag in a memory based on the status bit; and

responding to a poll request by an operating system.

7. (original) The method of claim 6 wherein responding comprises:

reading the flag from the memory.

8. (original) The method of claim 4 wherein servicing the interrupt comprises:

servicing the interrupt generated by the drive.

9. (original) A method comprises:

checking a status bit in response to an interrupt generated by a polling circuit in a chipset, the polling circuit detecting insertion of a medium into a drive;

updating a flag in a memory based on the status bit; and

responding to a poll request by an operating system.

10. (original) The method of claim 9 wherein responding comprises:

reading the flag from the memory.

11. (original) The method of claim 9 wherein checking the status comprises:

checking the status bit set by the polling circuit upon detecting the insertion of the medium.

12. (original) The method of claim 9 further comprises:

loading a program on the medium into a memory; and

executing the program.

13. (original) A computer program product comprising:

a machine useable medium having computer program code embedded therein, the computer program product having:

computer readable program code to configure a mode word;

computer readable program code to detect insertion of a medium into a drive based on the mode word; and

computer readable program code to start a program on the medium when the insertion is detected.

14. (original) The computer program product of claim 13 wherein the computer readable program code to configure the mode word comprising:

computer readable program code to configure the mode word in one of first, second, third, and fourth modes.

15. (original) The computer program product of claim 13 wherein the computer readable program code to detect the insertion comprises:

computer readable program code to periodically poll the drive when the mode word is configured in the first mode.

16. (original) The computer program product of claim 13 wherein the computer readable program code to detect the insertion comprises:

computer readable program code to service an interrupt indicating the insertion of the medium when the mode is configured in one of the second, third, and fourth modes.

17. (original) The computer program product of claim 13 wherein the computer readable program code to service the interrupt comprises:

computer readable program code to service the interrupt generated by a polling circuit in a chipset when the mode is configured in one of the second and third modes, the polling circuit detecting the insertion of the medium.

18. (original) The computer program product of claim 17 wherein the computer readable program code to service the interrupt comprises:

computer readable program code to check a status bit set by the polling circuit when the mode is configured in the second mode;

computer readable program code to update a flag in a memory based on the status bit; and

computer readable program code to respond to a poll request by an operating system.

19. (original) The computer program product of claim 18 wherein the computer readable program code to respond comprises:

computer readable program code to read the flag from the memory.

20. (original) The computer program product of claim 16 wherein the computer readable program code to service the interrupt comprises:

computer readable program code to service the interrupt generated by the drive.

21. (original) A computer program product comprising:

a machine useable medium having computer program code embedded therein, the computer program product having:

computer readable program code to check a status bit in response to an interrupt generated by a polling circuit in a chipset, the polling circuit detecting insertion of a medium into a drive;

computer readable program code to update a flag in a memory based on the status bit; and

computer readable program code to respond to a poll request by an operating system.

22. (original) The computer program product of claim 21 wherein the computer readable program code to respond comprises:

computer readable program code to read the flag from the memory.

23. (original) The computer program product of claim 21 wherein the computer readable program code to check the status bit comprises:

computer readable program code to check the status bit set by the polling circuit upon detecting the insertion of the medium.

24. (original) The computer program of claim 21 further comprising:

computer readable program code to load a program on the medium into a memory; and

computer readable program code to execute the program.

25. (original) A system comprising:

a processor;

a chipset coupled to the processor to control a drive; and

a memory coupled to the processor to store instruction code, the instruction code, when executed by the processor, causing the processor to:

configure a mode word,

detect insertion of a medium into a drive based on the mode word, and

start a program on the medium when the insertion is detected.

26. (original) The system of claim 25 wherein the instruction code causing the processor to configure the mode word causes the processor to:

configure the mode word in one of first, second, third, and fourth modes.

27. (original) The system of claim 25 wherein the instruction code causing the processor to detect insertion causes the processor to:

periodically poll the drive when the mode word is configured in the first mode.

28. (original) The system of claim 25 wherein the instruction code causing the processor to detect insertion causes the processor to:

service an interrupt indicating the insertion of the medium when the mode is configured in one of the second, third, and fourth modes.

29. (original) The system of claim 25 wherein the instruction code causing the processor to service the interrupt causes the processor to:

service the interrupt generated by a polling circuit in the chipset when the mode is configured in one of the second and third modes, the polling circuit detecting the insertion of the medium.

30. (original) The system of claim 29 wherein the instruction code causing the processor to service the interrupt causes the processor to:

check a status bit set by the polling circuit when the mode is configured in the second mode;

update a flag in a memory based on the status bit; and

respond to a poll request by an operating system.

31. (original) A system comprising:

a processor;

a chipset coupled to the processor to control a drive, the chipset having a polling circuit to detect insertion of a medium into the drive; and

a memory coupled to the processor to store instruction code, the instruction code, when executed by the processor, causing the processor to:

check a status bit in response to an interrupt generated by the polling circuit when the insertion is detected,

update a flag in a memory based on the status bit, and

respond to a poll request by an operating system.

32. (original) The system of claim 31 wherein the instruction code causing the processor to respond causes the processor to:

read the flag from the memory.

33. (original) The system of claim 31 wherein the instruction code causing the processor to check the status bit causes the processor to:

check the status bit set by the polling circuit upon detecting the insertion of the medium.

34. (currently amended) The system of claim 31 wherein the instruction code further causing the processor to:

~~locate~~ load a program on the medium into a memory; and

execute the program.